Abstract. The semiconductor industry continues to fabricate integrated circuits (ICs) with faster clock speeds, increased numbers of transistors, and smaller feature sizes. A complete set of the attributes describing a new technology generation (or node) is specified by an important features size such as the ½ pitch of the first level of metal lines in a dynamic random access memory (DRAM). Historically, Moore’s law has been used to describe the timing associated with the three-year cycle of new generations of memory devices. Recently, the introduction of new generations of logic devices has surpassed the three-year node cycle of memory devices. New technology generations have another significance. Each generation requires a new set of manufacturing equipment and, recently, new materials. The International Technology Roadmap for Semiconductors (ITRS) describes the technology requirements for volume manufacturing of integrated circuits (ICs) for each new technology node over the next 15 years [1]. In the 15-year horizon of the current ITRS, industry experts are considering the possibility of a revolution in microelectronics. The ITRS predicts that the gate length of transistors at the end of the roadmap will be less than 10 nm. The ITRS also discusses the need to move beyond traditional planar CMOS during the next 15 years and the potential need to move into revolutionary technologies at the end of the roadmap. The physical properties of materials change from bulk-like into “nano-like.” For example, on-chip interconnects will have dimensions that have nanowire properties. The development and manufacture of new generations of ICs or their successors will require new measurement technology. There will be many different challenges for metrology over the next 15 years. This paper describes these challenges.
INTRODUCTION

The timing of research, development, and manufacturing for leading edge integrated circuit manufacturing is shown in Figure 1. In order to develop processes for the 65 nm node, process and metrology tool purchase specifications have been agreed to, and suppliers have already begun development of capability. That means that the metrology community should have already begun research for the 45 nm node. Feature sizes for the 45 nm node are predicted to be below 20 nm for microprocessor linewidths.

The 2003 ITRS is expected to discuss the use of silicon on insulator (SOI) substrates as a key part of the transition from CMOS to future technologies [2]. It is likely that transistors fabricated on SOI having very thin silicon layers will be used in the next 15 years. The impact of SOI wafers on metrology is already significant. The detection of small particles on SOI wafers is degraded over that of polished silicon wafers. Measurement of film thickness as well as defect detection will all be more difficult.

In this paper, the needs and limits of metrology technology will be discussed. The IC process control precisions and process tolerances (ranges) predicted in the ITRS will be considered the motivating requirements for metrology. The metrology needs for Lithography, Transistor, and Interconnect processes will be individually described. One example is the discussion of critical dimension (CD) measurement limits of scanning electron microscopy (SEM), optical scatterometry, and atomic force microscopy (AFM) along with the potential role of high voltage CD-SEM in overcoming some of these issues. Another example is the measurement and control of interfaces such as those between the gate dielectric and the substrate silicon continue to be difficult at present dimensions and will become a bigger issue in the future. Advances in materials characterization methods such as transmission electron microscopy and new methods such as local electrode atom probes also will be discussed.

The paper will end with a look at the impact of shrinking feature dimensions on materials properties. All measurement methods require models for interpreting the signals received during sample analysis. The basic assumptions used in these models must change as feature dimensions shrink. Some examples of this will be provided.

LITHOGRAPHY METROLOGY

Wafer CD Metrology

We begin the discussion of lithography metrology with a description of the challenge presented by the requirements for critical dimension measurement at the end of a 15-year horizon. For the purposes of argument, it is useful to consider the polysilicon transistor gate used today to instead be a single crystal of silicon over its width. A 10 nm silicon CMOS gate would be less than 20 unit cells or less than 40 atomic layers wide. CD measurements are done by averaging the linewidth over some length of the transistor gate [3]. The measurement precision (6σ) to process tolerance ratio is defined as follows: (P/T) = 6σ/(0.2 × 10 nm). At a gate length of 10 nm and a process range of 10% (3σ) (total process range of 20%), the precision will be < 1 nm. Lithography process specifications in the ITRS use a P/T = 20%. We elaborate on the statistical process control based concept of P/T below. The 6σ precision for a 10 nm gate length is an incredible 0.4 nm. The precision amounts to less than one crystal lattice constant or four lattice planes along the (100) direction. Local atomic variations in linewidth can be overcome only when averaged CD measurements are made. Another issue is the impact of line edge roughness on the precision of the CD measurement as well as on the electrical properties of the transistor.

It is important to note that precision of the metrology tool also defines its resolution. Resolution is ability to distinguish between different values in the process range such as a 99 nm CD from 100 nm CD. This concept has been incorrectly ascribed to the ITRS, but it is based on established concepts from statistical process control. The resolution is the ability of a metrology tool to see differences in the process variable being measured. It is important to note that the P/T and C_p metrics do not address the need for a measurement to be statistically representative of process variation in the area being measured. Many measurements provide local data on a single (or a few) isolated features. This information may not represent process variation across a die. A metric for the statistical significance of a measurement method needs to be developed.

The above discussion assumes that the devices used in 15 years will resemble a traditional CMOS transistor. If that is true, the physical properties of materials at these dimensions and shapes will be those of a nano-wire and not bulk-like. These changes mean that the fundamental interaction of the measurement probe with the transistor gate is different. The dielectric function of a one-dimensional material is different from that of a bulk material. Maintaining transistor
performance at required leakage currents will require the use of SOI substrates. If other transistor designs are used, then CD and overlay metrology will certainly be impacted. Vertical transistors might utilize film thickness metrology instead of linewidth measurement to control CD.

In 2003, CD-SEM, scatterometry, and CD-AFM are all used for CD measurements in process development, and scatterometry and CD-SEM are both used for manufacturing control. Each technology has significant limitations, and none of them are considered capable of meeting a 10% P/T specification. Each method provides fundamentally different information about the process. Although both methods typically use test structures, CD-SEM can directly measure the feature of interest. CD-SEM determines the average linewidth over some section of the line while scatterometry determines the average linewidth of the many lines contained in the test structure over the width of the test structure. Thus, CD-SEM and scatterometry control fundamentally different aspects of a process. Here, we assume that the die level and wafer level distributions of linewidth are gaussian. CD-SEM is measuring one linewidth from the local distribution, and scatterometry is measuring the average (midpoint of a symmetric gaussian) of the distribution. A key need is to determine how many lines CD-SEM needs to measure in order to determine the average local linewidth. The issue for CD-SEM is that measurement of additional features decreases throughput. High throughput is an important need for manufacturing. In process development, changes in individual linewidth as well as the average, standard deviation, and range of linewidths are monitored. In manufacturing, usually one is interested in controlling the linewidth inside a desired process range across a die, on a wafer, and from wafer to wafer. The concepts described above are summarized in Figure 2. The diameter and area of contacts and vias are also controlled using critical dimension metrology. In 2002, only CD-SEM was capable of providing process control during volume manufacturing of contacts and vias. Thus, one can see that none of the available metrology methods provides metrology capability that meets the ITRS goals for all CD measurements.

![Figure 2](image2.png)

**FIGURE 2.** The concepts associated with the distribution of linewidths in a die and across a wafer are shown.

A number of experts believe that higher voltage CD-SEM is the only electron beam method that will be available and capable of meeting the requirements for the 45 nm node [4]. Previously, Joy [5] and others have stated that CD-SEMs can optimize two of three different properties: resolution, depth of field, and operating voltage. The lens designs used in CD-SEMs have resulted in a reduction in depth of field for several years. One way of overcoming this issue is the use of higher voltage systems. Since transmission electron microscopes (TEMs) and scanning-TEMs have been available for many years, the critical technology required for higher voltage CD-SEM is already known. The key issue is that of sample damage. Mizuno has been investigating the capabilities and consequences of higher voltage CD-SEM [6]. The biggest roadblock to use of high voltage CD-SEM may be the perception that higher voltage always damages samples. That perception is based mainly on the damage expected from use of a 10 to 20 keV beam. A second limit for SEM-based measurement is more fundamental to an electron beam based method.

Joy has also reminded us that there is an ultimate limit to CD-SEM linewidth measurement given by the range of the secondary electrons for SiO_2 (5 nm) and for crystalline Si (3 nm) [7]. This limit is based on the broadening of the secondary electron signal from an infinitely narrow beam as it scans over the edge of a line. The signal from the line edges overlap when the line is narrow enough as shown in Figure 3. Line edges were observed by the increase in secondary electron intensity shown in Figure 3 as the electron beam scanned over the edge of a line having a rectangular cross-section. Empirical algorithms are used to determine the location of line edge from the secondary electron signal. This signal is a function of the slope and shape of the sidewall as shown in Figure 4. When the line cross-section is not rectangular, the overlap occurs before the projected 5 nm limit as shown in Figure 5. Leading edge manufacturers are already
facing this issue due to the rounded edges at the top of lines formed in resist for sub 60 nm isolated lines. Algorithms aimed at producing CD values that match cross-sectional SEM values have already been developed. Despite this progress, the ~ 5 nm linewidth limit for CD-SEM is a reasonable estimation of the ultimate limit for CD-SEM.

FIGURE 3. The ultimate limit of CD-SEM is illustrated. The secondary electron intensity rises as the electron beam scans over the line edge. These plumes of increased intensity overlap as feature size decreases. The limit of CD -SEM is based on Secondary Electron resolution is \( \zeta \) the range of secondary electrons in the material.

FIGURE 4. The effect of sidewall angle on the secondary electron intensity of a CD-SEM line scan is shown. Figure courtesy Andras Vladar.

Scatterometry is also challenged by the rapid decrease in feature size. Scatterometry determines the average linewidth and shape of a test structure known as a grating. Although a number of different approaches to scatterometry are commercially available, all of them are based on one of the two main methods. One method uses a single wavelength and measures specular scatter intensity over a range of angles. The other uses an ellipsometer or reflectometer and measures the wavelength dependence of light scatter at a single angle. The most important recent development is the availability of software that determines linewidth and shape based on the data instead of comparing them to a library. Although the limits of scatterometry are not well characterized, Terry has proposed some general trends in the sensitivity of scatterometry to lineshape and linewidth changes [8]. In general, line shape changes impact the signal observed at ultraviolet (UV) wavelengths while linewidth impacts the signal observed in the visible wavelength range. The possibility of using infra-red wavelengths should be investigated.

The advent of “real time” scatterometry is an important breakthrough. “Real time” scatterometry calculates linewidth and shape instead of looking up a value from a fixed library of potential widths and shapes. It is now possible to evaluate the precision of the measurement without the issue of forcing the linewidth into a fixed set of potential values. If the
library contains linewidth variations that are larger than the required sensitivity to CD change, then precision may appear to be better than its true value.

The need for improved probe tips for AFM is well documented [9]. Carbon nanotubes are being explored as a potential tip for CD measurement of smaller features. The nanotubes are grown on the tips of AFM probes as shown in Figure 6. AFM has served the role of a reference measurement system.

FIGURE 6. Carbon nanotube probe tips for atomic force microscopy may extend CD-AFM to future technology nodes. Reproduced with permission from the NASA Aimes Center for Nanotechnology.

Mask CD Metrology

Since the features on a mask are larger than those printed on the wafer, the CD measurement challenges come from the materials used to construct the mask. The glass mask substrates are transparent at the wavelength used in the lithography exposure tool. Chrome metal features are used to block the light and form the desired features. Prior to the use of phase shifting and optical proximity correction (OPC), mask features were four times larger than those printed on the wafer [10]. The phase shift effect occurs when the chrome features have a specific height that changes the phase of the light relative to the light pass in other areas of the mask. For the purposes of this discussion, the phase shifting and OPC features are considered to be twice the dimensions of the smallest feature on the wafer. Masks that do not use phase shifting or OPC are referred to as binary masks. It is important to note that masks for optical lithography (including wavelengths from I-line, 193 nm, and 157 nm) use a pellicle (thin cover) located above the mask to keep contamination off of the mask surface. The pellicle results in two different needs that characterize mask CD measurement. At the place of mask fabrication (the mask shop), the CD variation can be measured before the pellicle is put in place. Since only the mask shops put pellicles (including replacing a pellicle) on the masks, CD measurements at the site of IC manufacture must measure the CD with the pellicle in place. Only optical methods can accomplish this. Another feature of masks is their shape. Wafers are circular, and masks are square. This means that the sample holder in the metrology tool is different for masks and wafers.

Optical microscopy-based measurement was able to provide CD control when feature sizes were larger. Now, CD-SEM must be used. CD-AFM can also measure feature dimensions on masks, especially the height of phase shifting features. Near term, the most critical need is for improved charge compensation for CD-SEM measurements. A number of methods can be used to overcome electron beam induced charging. One proposal is to use a low pressure, inert gas environment during imaging.[11] The damage from the ionization of the inert gas must be assessed. Longer term, a new method is needed for measuring CD with the pellicle in place.

Several other measurement requirements deserve mention. One need is for measuring the position-dependent phase of light after passing through the mask [1]. The second is development of an Aerial Image Measurement System (AIMS) at 157 nm and after that at extreme ultraviolet (EUV) wavelengths. AIMS is used to find defects in the mask that appear only on the exposed wafer. The AIMS tool projects the image that a mask will make in the resist on a wafer using the same wavelength, illumination pattern, and numerical aperture as the stepper or scanner. The image is captured by an optical system that allows for digital analysis. The AIMS tool is capable of testing through-focus effects without printing on a wafer. It is important to note that many defects are observed only in the projected image from a mask. AIMS tools have been able to measure mask defectivity with the pellicle in place. The goal of development is to provide this capability for 157 nm and EUV AIMS. Other defects can be directly observed on the mask using defect detection methods adapted to the mask. The accelerated introduction of new generations of lithography capability,—i.e., 193 nm, 157 nm, then EUV—and low volume of mask equipment sales have resulted in a move away from actinic (at wavelength) inspection (defect review) of masks.

Masks for EUV lithography reflect light instead of transmitting it [12]. The materials that reflect light at 13 nm are specially fabricated multilayers with repeating film stacks at thicknesses required for reflection. Near atomic smoothness is a key
requirement. Measurement of CD on EUV masks can certainly be done using CD-SEM. It seems likely that pellicles will be used for EUV masks, and measurement of CD with the pellicle in place must be done in the reflection mode.

Masks for electron projection lithography (EPL) are yet another significant change in mask materials and technology. Electron transparent thin films must be used to make masks. Non-destructive measurement of mask properties will be difficult.

**Overlay Metrology**

The issues facing overlay metrology come from the target structures as well as the measurement systems. An excellent review of overlay metrology can be found in the paper by Sullivan [13]. Tighter overlay tolerances imposed by low contrast levels will drive the development of new overlay measurement technology. Optical or SEM methods along with scanning probe microscopy (SPM) are all under consideration. The need for new target structures has been suggested as a means of overcoming the issues associated with phase shift mask and optical proximity mask alignment errors not detectable with traditional targets.

**FRONT END PROCESSES (TRANSISTOR FABRICATION) METROLOGY**

Complementary metal oxide semiconductor (CMOS) transistors will continue to be used in leading edge devices in the near term [1]. CMOS-like structures using SOI substrates can extend CMOS perhaps to the end of the 15-year horizon of the roadmap. Higher dielectric constant gate dielectric materials and ultra-shallow junctions will be used to scale transistor dimensions while maintaining desired electrical properties. Silicon dioxide is no longer a viable material for leading edge ICs because of the high leakage current that occurs when the thickness decreases below 2 nm. Silicon oxynitride is providing a transition to higher dielectric constant materials as the search for a viable higher dielectric constant material continues. Hafnium oxide, hafnium silicates, and stacked layers of these materials are all coming closer to meeting the leakage current and transistor mobility requirements. In this section, the key challenges facing front end processes (FEP) metrology are described.

The challenges facing FEP metrology can be summarized in terms of the precision requirements for logic transistors at the 45 nm node [1]. The physical gate length of the transistors in high performance logic devices at the 45 nm node will be 18 nm, and the equivalent oxide thickness of the gate dielectric will be between 0.5 and 0.8 nm. For an equivalent oxide thickness of 0.5 nm, process range of ± 4%, and P/T ratio of 0.1 = \(6\sigma/(2*0.04*0.5 \text{ nm})\), the 3\(\sigma\) precision will be 0.002 nm equivalent oxide thickness (EOT) [14]. If the gate dielectric is composed from one material with a dielectric constant of 20, then the physical thickness of the 0.5 nm EOT will be \(\sim 0.5 \times 20/4 = 2.5 \text{ nm}\). The 3\(\sigma\) precision will then be \(\sim 0.002 \times (20/4) = 0.01 \text{ nm}\). Here, we used 4 instead of the exact value of the dielectric constant of silicon dioxide. Although meeting the challenges associated with measuring high \(\kappa\) film thickness with a precision of 0.01 nm is clearly difficult, the true nature of the film stacks provides a more difficult measurement requirement.

Optical and electrical measurements are both important means of controlling processes. Ellipsometry, capacitance-voltage (C-V) measurement, and non-contact C-V are all used for silicon oxynitride in present generation transistors. This is expected to continue for high \(\kappa\) gate stacks. The challenges facing each method are discussed below.

Optical modeling of the high \(\kappa\) film is a critical part of metrology. Although the Tauc–Lorentz form of the dielectric function has been successfully used to model high \(\kappa\) materials, it is available only in laboratory grade ellipsometers [15]. In-line optical metrology tools use damped Lorentz oscillators (or similar function forms) that require elaborate fitting of two or more oscillators to achieve the same function form as provided by the Tauc–Lorentz model. The dielectric function of a hafnium dioxide film is shown in Figure 7. The dielectric function is sensitive to process conditions as well as compositional changes such as the addition of alumina or silica [15]. It has been shown previously that measurement precision is a function of both the ellipsometer hardware and the optical model. Although functional forms for the dielectric function that have many fitting parameters will have better fit qualities, a significant loss of precision is possible [16]. That is why a single slab model of silicon dioxide is used instead of one that includes an interface layer [15].
The best available analysis of available high $\kappa$ materials indicates that an interface layer must be used below the high $\kappa$ layers. This interface layer provides a better match to the silicon channel area as well as separating the high $\kappa$ from the channel region. High $\kappa$ films seem to have defects and regions of charge that reduce electron and hole mobility in the channel. Although the physical thickness of the interface layer will be much less than that of the high $\kappa$ material, it will have a significant contribution to the total capacitance of the gate stack. The contribution of the interface layer to the total physical film thickness is $T_{\text{total}} = T_{\text{interface}} + T_{\text{high } \kappa}$, while the contribution to the electrical thickness as measured by the equivalent oxide thickness is $E\text{OT} = T_{\text{interface}} + T_{\text{high } \kappa}(3.9/\kappa_{\text{high } \kappa})$ [16]. Measuring and controlling the interface layer is complicated by both the short path-length for light and the absorption of light in the near UV and UV region of the spectrum. Jellison has provided an excellent analysis of why measurement of thin films is improved in the UV region of the spectrum [17].

A largely unappreciated issue is measurement of thin films on SOI substrates. The thickness of the silicon layer above the buried oxide is projected to decrease below 20 nm in the future. The ITRS roadmap for SOI top layer thickness for future technology nodes is shown in Figure 8 [18]. Extra reflections arise from the interfaces of the buried oxide layer. In addition, small changes in thickness uniformity for the top silicon layer may degrade the precision of the thickness measurement for the gate dielectric layer. There is another complication that remains somewhat unrecognized. The quantum confinement of carriers in ultra-thin SOI causes a shift in the band edge and a change in the shape of the band edge [18]. In other words, the wavelength-dependent optical constants change with film thickness. This can make optical modeling very difficult. The effective optical response of the SOI wafer includes the shifted optical constants of the top silicon, the buried silicon dioxide, and the bulk silicon constants. The optical constants of the top silicon layer will also be affected by the doping level especially in the IR. In Figure 9, the impact of different possible band edge shapes on the imaginary part of the dielectric function is shown for direct and indirect semiconductors. Recently, an effective dielectric stack approach has been used to optically model the SOI wafer [18].

**FIGURE 7.** The difference between the dielectric function of silicon dioxide and high $\kappa$ materials is shown. Light in the near UV and UV wavelengths is absorbed by high $\kappa$ materials as indicated by the values of the imaginary part of the dielectric function.

**FIGURE 8.** The ITRS for silicon on insulator wafers (SOI) for full depleted silicon (at maximum of thickness range) predicts the need for ultrathin silicon layers. It should be noted that SOI wafers are not available in enough quantity for volume production of IC for even the thickest SOI layer found in the ITRS.

**FIGURE 9.** The change in optical properties due to quantum confinement in ultrathin SOI is shown.
Electrical measurements can be done non-destructively after dielectric deposition (or growth) or after formation of a capacitor and/or transistor test structure. Electrical characterization of a dielectric layer can be done after depositing a fixed amount of charge using corona discharge methods [19]. The top layer of a traditional capacitor test structure can be either doped poly-silicon or a metal such as titanium nitride. Extraction of the EOT from C-V measurements of thin silicon dioxide or silicon oxynitride layers is possible after correction for charge depletion in the poly-silicon gate electrode, the quantum states at the silicon substrate–oxide interface, and minimization of the effects of leakage current. C-V measurement of the EOT of high κ materials is complicated by the high density of charge traps at the interface $D_{it}$. Hung and Vogel have shown that the error in EOT is $\sim 10\%$ when the $D_{it}$ is $\sim 10^{13}$ [20]. This effect is shown in Figure 10.

FIGURE 10. Effect of Dit on C-V measurement is shown. C-V data was simulated for a 1 nm oxide layer using a program developed at NIST. The simulated C-V curves were then characterized by the Hauser’s CVC program. a. When Dit = $1 \times 10^{10}$, the dielectric thickness was found to be $Tox = 1.19 +/- .03$ with an RMS Error = 3.0%; b. When Dit = $1 \times 10^{11}$, the dielectric thickness was found to be $Tox = 1.19 +/- .03$ with an RMS Error = 2.7%; c. When Dit = $1 \times 10^{12}$, the dielectric thickness was found to be $Tox = 1.19 +/- .03$ with an RMS Error = 2.3%; d When Dit = $1 \times 10^{13}$, the dielectric thickness was found to be $Tox = 0.78 +/- .05$ with an RMS Error = 10.8%.

Metrology for dopant dose and junction depth is considered to be capable of providing adequate process control in the near term [21]. Measurements such as ellipsometric determination of gate dielectric thickness are often done using test structures placed on the scribe lines (also called kerf) between the die. In order to get more die on a wafer, the scribe lines and thus the test structure size are shrinking. This change impacts two aspects of a measurement. First, the metrology tool must be redesigned so that the spot size of the measurement safely fits into the test structure. The second impact is that the averaging over the measurement spot size may be greatly reduced. At some point, the test structure size could shrink to the size that makes the resultant value not representative of the measured feature inside the die. Another aspect of test structures is that metrologists consider the kerf structure to be too different from the same structure inside a die to be representative of the actual property being measured.
INTERCONNECT METROLOGY

Copper interconnect technology has been used in commercially available ICs for several years. Copper-Damascene processing will continue to be used for the next several technology nodes. The main change will be the use of successively lower dielectric constant insulator layers and thinner barrier layers. The ITRS had predicted a rate of decrease in dielectric constant of the interconnect insulator that was not achievable. The latest ITRS describes a more conservative path to lower \( \kappa \) values. The insulator layer is not the only materials issue facing interconnect. Copper metal lines were initially believed not to be prone to void formation from electro-migration. Therefore, it is important to note the reports of reliability issues as copper Damascene processing moved from the 180 nm node to the 130 nm node [22]. Stress in the barrier and copper layers resulted in electro-migration induced openings in copper lines. It is interesting to note that this problem seemed to be isolated to the ICs from a process flow that operated at the highest clock speeds. Metrology used during processing did not detect these potential issues. Process changes that reduced film stress have resulted in ICs that do not show this problem. Although in-line metrology for void detection was not yet available, voids may not have been present until the IC was tested. Micro-voids may agglomerate when the IC is heated by current flow during operation. In-line, high spatial resolution stress measurement may have predicted void formation. To date, the ITRS Interconnect Roadmap teams has not changed its prioritization of void detection metrology [23].

Interconnect metrology needs are based on control requirements for low \( \kappa \) deposition and patterning, metal deposition and copper plating, and chemical mechanical polishing. It is important to distinguish between the measurements that are routinely done during manufacturing and those done during materials and process development. Routine measurements during manufacturing include dielectric (and possibly barrier/copper) film thickness, trench and contact/via CD, and film flatness. The shortened product cycle has pushed some IC manufacturers to use processes that are not as mature as once possible. Another well known practice is the decrease in use of metrology as a new factory or new process flow matures. Thus, one can state only general rules concerning which metrology tools are used during manufacture.

The characterization of the effective \( \kappa \) value of the entire patterned metal interconnect structure is a critical part of process development. The bulk value of the dielectric constant represents the lower limit of the effective \( \kappa \). The etch stop and other layers used in the insulator stack as well as the barrier layer all interact to produce a process-dependent value of \( \kappa \) [24]. During process development, electrical test structures are used to test for the resistance–capacitance (RC) product. Interlocking comb as well as serpentine RC test structures are shown in Figure 11. These test structures play a critical role in the characterization of porous low \( \kappa \).

FIGURE 11. RC test structure for low \( \kappa \) interconnect.

Determination of pore size distribution and detection of “killer” pores remain key materials characterization needs that are potentially useful during manufacturing. Pore size distribution (PSD) has been characterized using diffuse x-ray scattering (small angle x-ray scattering), ellipsometric porosimetry (EP), positron annihilation spectroscopy, small angle neutron scattering, and high resolution transmission electron microscopy (HR-TEM) [25, 26, 27, 28]. Of these, diffuse x-ray scattering and ellipsometric porosimetry are under consideration for routine use at or in-line. Diffuse x-ray scattering provides information on the average pore size and the width of the distribution. It is possible to fit diffuse x-ray scattering data to several different model distributions as shown in Figure 12. Diffuse x-ray scatter is measured using x-ray reflectivity (XRR) systems with detector systems that collect the diffuse scatter. Thus, XRR data can also be obtained. XRR data are sensitive to an amazing variety of process conditions [28]. Multi-deposition with repeating deposition steps, process changes, and adhesion layers can all be observed as shown in Figure 13. Ellipsometric porosimetry is based on observation of the change in refractive index as gas is absorbed on the pore surfaces [26]. Reports of observation of bifurcated PSD with only minor amounts of one smaller pore size PSD seem to indicate a strength for EP. The absorption of toluene and other organic vapors may not make EP suitable for in-line measurement.
FIGURE 12. Measurement of pore size distribution by small angle x-ray scattering. The effect of different modeling parameters is shown. Figure courtesy Mathew Wormington.

FIGURE 13. X-ray reflectivity measurement of low $\kappa$ film stacks. XRR measurement has been found to be sensitive to the presence multi-layer structures. From work of William Chism, Long Vu, B. Kastenmeier, A. Knorr, and A. Diebold [29].

Void detection in copper lines has been a key interest for the interconnect community. Most methods are based on detecting a change in the total volume of copper in a patterned structure at different locations across a wafer. Although several methods seem capable of detecting 1% or less change in copper volume, the biggest issue is the variability in copper volume across a wafer and from wafer to wafer due to linewidth variation and variability in
chemical mechanical polishing. Metal Illumination and x-ray fluorescence have been proposed as potential solutions to this problem [30, 31]. The other approach would be detection of the magnetic field due to the current flow through the interconnect lines using magnetic force microscopy or through a SQUID detector [32, 33].

Several other materials characterization methods deserve mention. One new method that can be used during process development is the ultrasonic force microscope (UFM) [34]. UFM can be used to observe delamination, measure the elastic constants of low κ materials, and study pore size information [34]. The ability of UFM to observe killer pores should be investigated. The crystal structure and trace impurities in the barrier layer and copper lines can be studied with a new method known as local electrode atom probe, which is discussed below.

MATERIALS CHARACTERIZATION

Although there are a number of improvements and advances in materials characterization, this section will focus on only two: advanced transmission electron microscopy (TEM) and local electrode atom probe (LEAP). Both of these methods are moving toward the goal of an atom by atom look at small sample areas.

The advent of high angle–annular dark field (HA-ADF) detectors and greatly reduced probe size for scanning TEM have greatly advanced the resolution of interfacial characterization [35, 36, 37, 38]. A consensus method for measuring the thickness of thin dielectric layers was proposed in a recent paper discussing the difficulties associated with TEM-based characterization of interfacial layers [39]. The main issue for both HR-TEM and ADF-STEM is that both methods image a cross-section through a sample of finite thickness. This is shown in Figure 14. Both HR-TEM and ADF-STEM find the same value for dielectric layer thickness when each method is carefully applied to thin samples [39]. The use of wedge polished samples and HA-ADF-STEM was considered to be the most practical method of dielectric film thickness measurement. This method can be applied to 50 nm thick samples while HR-TEM requires the sample to be ~ 10 times thinner. As Batson has shown, active correction of lens aberration results in a smaller probe size and greatly improved resolution in ADF-STEM [35]. Other improvements in HR-TEM and ADF-STEM will come from the use of electron monochromators [40]. Muller has already shown the improvements that are possible in electron energy loss spectroscopy when more monochromatic electron beams are used [41]. Kisielowski has discussed the potential of a tomograph-like approach for HR-TEM. The goal is to develop the ability to produce atom by atom like maps [42].

Kelly and others have introduced the local electrode atom probe method [43]. Field ionization from pointed tips has been used to characterize crystalline structure for many years [43]. As shown in Figure 15, LEAP uses an electrode placed close to the tip surface to reduce the voltage required to produce high fields [42]. Because fields are lower, rapid pulsing of the electrode potential results in the ability to rapidly field ionize and thus analyze a sample. Recent results of interest to the semiconductor community include the location of boron atoms in doped silicon and the analysis and location of impurities in plated copper [44]. Although atomic planes can be observed when images are rotated to align along crystallographic directions, the detector efficiency of ~ 60% presently does not allow images showing all the atoms in local structures. Thus, crystallographic defects in silicon that can be observed by TEM methods are not presently observable in LEAP. Improvements in detector technology are one path to greater atomic level microscopy.
CHARACTERIZATION AND METROLOGY FOR EMERGING DEVICE TECHNOLOGIES

Molecular electronics, spintronics, nanowires, single electron, and nanotube devices are a few of the Emerging Technologies discussed in the 2001 ITRS [1]. In this section, the materials characterization methods used to characterize some of these devices are discussed along with other potentially useful methods and fabrication procedures. This section is not meant to be exhaustive, but rather it is meant to start the discussion between the metrology community and the emerging devices communities.

Molecular Electronics

Molecular electronics refers to the use of molecular assemblies that are mainly used as either transistor or capacitor replacements. Referring to Pease’s review [45], there are four aspects to molecular electronics. The first is design and fabrication of molecular switches onto a template. The use of crossed wires allows “tiling” in two dimensions [45] as shown in Figure 16. The molecular switches connect the upper and lower wires allowing each molecular switch to be individually addressed. There are a number of fundamental differences between transistors and two terminal devices. Transistors have gain while two terminal devices are dissipative. Another difference Pease discusses is that different tasks such as opening, closing, and reading are done using different wires while two terminal devices use different voltages. One type of two-terminal switch is the supramolecular complex. Examples include catenanes or rotaxanes, which are mechanically interlocking molecules that exhibit different positions relative to each other based on their oxidation state. The circuit switching voltage is the ionization energy plus the activation energy. Different conformations of these molecules have very different tunneling currents. The electrical properties of these new “molecular switches” require non-traditional testing. Another source of information used here is the publications of Weiss. Weiss is working on the chemical switching of molecular conductance [46, 47, 48]. As Weiss’s publications indicate, rapid scanning capability is a critical requirement for observation of dynamic phenomena such as molecular switching. All of these changes require a different metrology approach. The other three aspects in Pease’s review are architecture development, chemical assembly methods, and circuit multiplexing.

Although the overlapping wires shown in Figure 16 can be imaged using SEM, even a low resolution view of molecular structure cannot be observed. Weiss has observed conductance switching using scanning tunneling microscopy [46]. As shown in Figure 17, molecules appear as stick-like structures whose height changes. X-ray diffraction of crystals of molecular superstructures has been used to understand the atomic structure of these molecular superstructures [45]. Electrical testing and chemical analysis have been used to understand the oxidation state and function of molecular electronics structures [45]. UV–visible wavelength absorption spectroscopy has been used to confirm the conformational state and redox potential of [2]-catenane [45].

FIGURE 16. One example of molecular electronics. Molecular switches are formed between overlapping wires. Changes in the configuration of molecules result in changes in tunneling current allowing the molecule to act as a switch. Reproduced with permission from James Heath, Fraser Stoddart, and Anthony Pease.
FIGURE 17. Observation of the change in configuration of a molecular switch by scanning tunneling microscopy. a) The molecular structure of one type of organic molecule used undergoing switching. b) View of time dependent height of switching molecules observed by AFM. Reproduced with permission from Paul Weiss. See also references 46 and 47.

Nanowires and Nanocontacts

The term nanowire seems to represent a wide variety of shapes and thicknesses of wire-like materials. Often, the nanowire dimensions are greater than those found in leading edge copper interconnects. The interesting aspect of nanowires includes their conduction and magnetic properties. If the nanowire is thin enough, quantum confinement in two dimensions results in new properties. The pioneering work of Takayanagi [49, 50, 51, 52] on gold and silicon nanowires illustrates both the interesting nature of nanowires and the materials characterization that is being used to observe these properties. Gold nanowires that were one to several atoms thick were observed in a specially prepared TEM. These nanowires showed quantized conductance (G) in units of $2e^2/h = G_0$ based on the number of atoms in the diameter of the wire [49, 50, 51]. Here, $e$ is the electron charge, and $h$ is Plank’s constant. Helical gold and silicon nanowire structures were also studied experimentally and theoretically [50, 51, 52]. The quantized conductance was found to be temperature-dependant [51, 52]. Some workers have predicted that structural integrity and quantized conductance will begin to be observed when the number of atoms in the cross-section is ~130 or less [53]. In fact, the radius of the nanowire can be calculated from the measured conductance using the semiclassical expression for the conductance [52]: $G/G_0 = (\kappa_f R/2)^2 (1 - 2/(\kappa_f R))$. Here, $\kappa_f$ is the bulk metal Fermi wavevector, and $R$ is the radius of the nanowire. Thus, the measurement of conductance is a key materials characterization method. Special electrical testing methods have been reported in the literature [54]. Frequently, formation of long nanowires of near atomic thickness is difficult, and indentation methods are used to form point contacts [53].

Korgel and co-workers have grown 4 to 5 nm wide silicon nanowires using alkanethiol-coated gold nanocrystals of 2.5 nm in diameter [55]. The crystallographic orientation of these silicon nanowires was controlled by the reactant gas pressure [55]. TEM and electron diffraction characterization required the use of chloroform to extract the nanowires onto a standard sample holder. These nanowires have small enough diameters to exhibit the effects of quantum confinement (and possibly new surface states) in photoluminescence and absorption spectra [55]. The absorption edge was blue shifted from the indirect band edge of 1.1 eV of bulk Si and showed discrete absorbance features. Silicon nanowires oriented along the $<100>$ direction showed absorbance features considered to be similar to the L to L critical point of bulk Si, while $<110>$ oriented nanowires showed molecular like transitions [55]. The band edge shift of the 2D confined electrons in silicon nanowires can be understood using the same ideas discussed above in the 1D confinement of the top layer of silicon in SOI wafers [18].

Larger nanowires have also been studied by a great number of workers, and only a few examples are used here to illustrate certain principles [56, 57, 58, 59, 60]. 15 to 35 nm wide silicon nanowires have been fabricated using non-lithographic methods by Heath and co-workers [57, 58]. Specifically, silicon
nanowires were fabricated using Au or Zn particle catalyzed chemical vapor deposition (CVD) of silane gas [57, 58]. The nanowires were then placed on three lithographically formed terminal test structures. The transport properties were characterized using current–voltage measurements of these wires, and SEM, TEM, and AFM were used to characterize the structure of the anowires [57, 58]. Bismuth nanowires have been formed using lithographic methods, and the unusual band structure of bismuth along with the confinement in thin wires results in transport properties becoming semiconducting and, at lower temperatures, insulating [59]. These wires did not exhibit quantized conductance. Lieber and co-workers have also fabricated boron or phosphorous doped silicon nanowires that were greater than 50 nm in diameter [60]. This group studied the temperature dependence of current–voltage properties. The wires exhibited reduced carrier mobility, and doping resulted in the expected p- or n-type behavior [60].

The fabrication methods used in the study of nanowires may provide the means of making reference and test materials for CD measurements before lithography methods used in volume manufacturing are available. From the above discussion of nanowires, it is clear that both physical and electrical characterization methods are critical to thorough characterization. In this light, Diebold, Chism, and Joy have proposed several approaches to nanowire characterization that result in simultaneous extraction of both physical and electrical properties. TEM electron holography has been used to observe the phase shift in electrons due to the electron present in a nanowire carrying a small current. If the nanowire has a small enough diameter and is at an appropriate temperature, it should exhibit quantized conduction. Using the shift in the electron phase in TEM holography, the average wire thickness can be compared to the diameter (= thinnest part of the nanowire) calculated from the quantized conductance. and magnetic force microscopy as means of quantifying nanowire dimensions [61] . This method requires a specially modified TEM that allows nanowire manipulation similar to Takayanagi’s group but includes the ability to do holography. Another approach would be to build test structures that have a complete current loop with one part of the loop having the nanowire. One can study the temperature-dependent current through the nanowire by observing the shift in frequency of a “tapping” magnetic force microscope [61].

CONCLUDING REMARKS

The status and challenges facing silicon semiconductor metrology have been reviewed. Microscopy for critical dimension measurement and other applications remains the most important long-term challenge facing the industry. As new technologies such as molecular electronics, nanowires, and spintronics are being explored, potential uses for next generation silicon semiconductor devices should be explored.

ACKNOWLEDGEMENTS

The author would like to thank many folks in the metrology community who have shared their insights. I thank Will Chism and P.Y. Hung for discussions about FEOL and BEOL metrology. I thank Will Chism for discussions about scatterometry for CD. Peter Zeitzoff and Howard Huff have provided all of us with a vision of how CMOS can be extended into the future with new materials and SOI substrates. David Joy has continued to provide insights into SEM and TEM science and technology. I thank Professor Takayanagi for sending me a copy of his inspiring video on gold and silicon nanowires. I credit the presentations and discussions of Jim Heath and Paul Weiss for inspiration about molecular electronics. I thank Dave Muller, Steve Pennycook, Christian Kisielowski, Suzanne Stemmer, and Brendan Foran for enlightening discussions on TEM and STEM.

REFERENCES

6. F. Mizuno, S. Yamada, and T. Ono, “Effects of 50 to 200-keV Electrons by BEASTLI Method on
8. F. Terry, private communication.
21. A.C. Diebold, “Metrology requirements over the next 15 years,” ECS Proceedings, in process.


41. D. Muller, private communication.

42. C. Kisielowski, private communication.


44. T.F. Kelly, private communications.


